SYNERGY POLYTECHNIC, BBSR

The Lesson Plan

Descipline: computer science engineering	Semester: 3rd sem	Name of the Teaching Faculty: Tapaswend Raut
Subject: computer system Architecture	No of Days/per week class allotted: 4	Semester from Date: to Date: No of Weeks: 15 1.7.24 18.11.24
Week	Class Day	Theory/Practical Topics
1st	1st	Chap-1 Basic structure of computer hardware
	2nd	Functional units
	3rd	computer components
	4th	Performance measures
	5th	
2nd	1st	Memory addressing & operations
	2nd	continuing memory addressing & operations
	3rd	Chap-2 Fundamentals to Instructions
	4th	Operands and Op codes
	5th	
3rd	1st	Instruction formats
	2nd	continuing instruction formats, Addressing modes
	3rd	continuing addressing modes
	4th	continuing addressing modes
	5th	
4th	1st	Chap-3 Register Files
	2nd	continuing Register Files
	3rd	complete instruction execution
	4th	continuing complete instruction execution
	5th	
5th	1st	Hardware control
	2nd	continuing Hardware control
	3rd	continuing Hardware control
	4th	Micro Program control
	5th	

Tapaswend Raut
Sign of Faculty

HOD 10/6/24

Principal 10/6/24

SYNERGY POLYTECHNIC, BBSR

The Lesson Plan

Discipline: computer science engineering	Semester: 3rd	Name of the Teaching Faculty: Tapaswini Raut
Subject: computer system Architecture	No of Days/per week class allotted: 4	Semester from Date: 1.7.24 to Date: 18/11/24 No of Weeks: 15 15

Week	Class Day	Theory/Practical Topics
1st	1st	continuing Microprogram control
	2nd	continuing Microprogram control
	3rd	chap 4 Memory characteristics
	4th	Memory hierarchy
	5th	
2nd	1st	continuing Memory hierarchy
	2nd	RAM and ROM organization
	3rd	RAM and ROM organization continuing
	4th	Interleaved Memory
	5th	
3rd	1st	Cache Memory
	2nd	continuing Cache Memory
	3rd	Virtual Memory
	4th	continuing Virtual Memory
	5th	
4th	1st	chap 5 Input - Output Interface
	2nd	Modes of data transfer
	3rd	continuing modes of data transfer
	4th	Programmed I/O transfer
	5th	
5th	1st	continuing programmed I/O transfer
	2nd	Interrupt driven I/O
	3rd	continuing Interrupt driven I/O, DMA
	4th	continuing DMA
	5th	

Tapaswini Raut
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HOD

Principal 10/8/24

SYNERGY POLYTECHNIC, BBSR

The Lesson Plan

Descipline: computer science engineering	Semester: 3rd	Name of the Teaching Faculty: Taparswini Raut
Subject: computer system Architecture	No of Days/per week class allotted: 4	Semester from Date: 1.7.24 to Date: 18.11.24 No of Weeks: 15

Week	Class Day	Theory/Practical Topics
1st	1st	I/O Processor
	2nd	continuing I/O Processor
	3rd	Chap 6 Bus and System Bus
	4th	Types of system Bus
	5th	
2nd	1st	continuing Types of system Bus
	2nd	Bus Structure
	3rd	continuing Bus Structure
	4th	Basic Parameters of Bus design
	5th	
3rd	1st	SCSI
	2nd	continuing SCSI
	3rd	USB
	4th	continuing USB
	5th	
4th	1st	Chap 7 Parallel Processing
	2nd	Linear Pipeline
	3rd	continuing Linear Pipeline
	4th	Multiprocessor
	5th	
5th	1st	continuing Multiprocessor
	2nd	Flynn's classification
	3rd	continuing Flynn's classification
	4th	
	5th	

Taparswini Raut
Sign of Faculty

HOD

Principal 10/6/24