SYNERGY POLYTECHNIC, BBSR

The Lesson Plan

Descipline:CSE	Semester:3rd	Name of the Teaching Faculty:Saswati sanghamitra Pradhan
Subject:DIGITAL ELECTRONICS	No of Days/per week class allotted:4	Semester from Date: 1.7.24 to Date: 18.11.24 No of Weeks: 15
Week	Class Day	Theory/Practical Topics
1st	1st	**Unit-1: Basics of Digital Electronics** Number System-Binary, Octal, Decimal, Hexadecimal - Conversion from one system to another number system.
	2nd	Arithmetic Operation-Addition, Subtraction, Multiplication, Division, 1"s & 2"s complement of Binary numbers& Subtraction using complements method
	3rd	Digital Code & its application & distinguish between weighted & non-weight Code, Binary codes, excess-3 and Gray codes.
	4th	Logic gates: AND,OR,NOT,NAND,NOR, Exclusive-OR, Exclusive-NOR--Symbol, Function, expression, truth table & timing diagram
2nd	1st	Universal Gates& its Realisation
	2nd	Boolean algebra, Boolean expressions, Demorgan"s Theorems
	3rd	Represent Logic Expression: SOP & POS forms
	4th	Karnaugh map (3 & 4 Variables)&Minimization of logical expressions ,don"t care conditions
	5th	Revision/Numericals
3rd	1st	Karnaugh map (3 & 4 Variables)&Minimization of logical expressions ,don"t care conditions
	2nd	Karnaugh map (3 & 4 Variables)&Minimization of logical expressions ,don"t care conditions
	3rd	Karnaugh map (3 & 4 Variables)&Minimization of logical expressions ,don"t care conditions
	4th	Karnaugh map (3 & 4 Variables)&Minimization of logical expressions ,don"t care conditions
	5th	Revision/Numericals
4th	1st	**Unit-2: Combinational Logic Circuits** Half adder, Full adder
	2nd	Half Subtractor, Full Subtractor
	3rd	Serial and Parallel Binary 4 bit adder.
	4th	Multiplexer (4:1), De- multiplexer (1:4),
	5th	Revision/Numericals
5th	1st	Decoder, Encoder,
	2nd	Digital comparator (3 Bit)
	3rd	Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above)
	4th	Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above)
	5th	Revision/Numericals

Saswati S Pradhan
Sign of Faculty 11/06/2024

HOD 11/6/2024

Principal 11/6/24

SYNERGY POLYTECHNIC, BBSR

The Lesson Plan

Descipline:CSE	Semester:3rd	Name of the Teaching Faculty: Saswati sanghamitra Pradhan
Subject:DIGITAL ELECTRONICS	No of Days/per week class allotted:4	Semester from Date: 1.7.24 to Date: 18.11.24 No of Weeks:15
Week	Class Day	Theory/Practical Topics
1st	1st	Revision/Numericals
	2nd	Revision/Numericals
	3rd	Revision/Numericals
	4th	Revision/Numericals
	5th	Revision/Numericals
2nd	1st	**Unit-3: Sequential logic Circuits** Principle of flip-flops operation, its Types,
	2nd	SR Flip Flop using NAND,NOR Latch (un clocked)
	3rd	Clocked SR,D,JK,T,JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications
	4th	Clocked SR,D,JK,T,JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications
	5th	Revision/Numericals
3rd	1st	Clocked SR,D,JK,T,JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications
	2nd	Clocked SR,D,JK,T,JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications
	3rd	Clocked SR,D,JK,T,JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications
	4th	Clocked SR,D,JK,T,JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications
	5th	Revision/Numericals
4th	1st	Concept of Racing and how it can be avoided.
	2nd	Concept of Racing and how it can be avoided.
	3rd	Revision/Numericals
	4th	Revision/Numericals
	5th	Revision/Numericals
5th	1st	Unit-4: Registers, Memories & PLD
	2nd	Shift Registers-Serial in Serial -out, Serial- in Parallel-out, Parallel in serial out and Parallel in parallel out
	3rd	Universal shift registers-Applications.
	4th	Types of Counter & applications
	5th	Revision/Numericals

Saswati S Pradhan
Sign of Faculty 11/06/2024

HOD 11/6/2024

Principal 11/6/24

SYNERGY POLYTECHNIC, BBSR

Lesson Plan

cipline:CSE	Semester:3rd	Name of the Teaching Faculty: Saswati sanghamitra Pradhan
ject:DIGITAL ELECTRONICS	No of Days/per week class allotted:4	Semester from Date: 1.2.24 to Date: 18.4.24 No of Weeks:15
ek	Class Day	Theory/Practical Topics
1st	1st	Binary counter, Asynchronous ripple counter (UP & DOWN), Decade counter. Synchronous counter, Ring Counter.
	2nd	Binary counter, Asynchronous ripple counter (UP & DOWN), Decade counter. Synchronous counter, Ring Counter.
	3rd	Concept of memories-RAM, ROM, static RAM, dynamic RAM,PS RAM
	4th	Concept of memories-RAM, ROM, static RAM, dynamic RAM,PS RAM
	5th	Revision/Numericals
2nd	1st	Basic concept of PLD & applications
	2nd	**Unit-5: A/D and D/A Converters** Necessity of A/D and D/A converters.
	3rd	D/A conversion using weighted resistors methods
	4th	D/A conversion using R-2R ladder (Weighted resistors) network.
	5th	Revision/Numericals
3rd	1st	A/D conversion using counter method.
	2nd	A/D conversion using counter method.
	3rd	A/D conversion using Successive approximate method
	4th	A/D conversion using counter method.
	5th	Revision/Numericals
4th	1st	**Unit-6: LOGIC FAMILIES** Various logic families &categories according to the IC fabrication process
	2nd	Various logic families &categories according to the IC fabrication process
	3rd	Various logic families &categories according to the IC fabrication process
	4th	Characteristics of Digital ICs- Propagation Delay, fan-out, fan-in, Power Dissipation ,Noise Margin ,Power Supply requirement &Speed with Reference to logic families.
	5th	Revision/Numericals
5th	1st	Characteristics of Digital ICs- Propagation Delay, fan-out, fan-in, Power Dissipation ,Noise Margin ,Power Supply requirement &Speed with Reference to logic families.
	2nd	Characteristics of Digital ICs- Propagation Delay, fan-out, fan-in, Power Dissipation ,Noise Margin ,Power Supply requirement &Speed with Reference to logic families.
	3rd	Features, circuit operation &various applications of TTL(NAND), CMOS (NAND & NOR)

	4th	Features, circuit operation &various applications of TTL(NAND), CMOS (NAND & NOR)
	5th	Features, circuit operation &various applications of TTL(NAND), CMOS (NAND & NOR)

Saswati S Radhan
Sign of Faculty 11/06/2024

HOD 11/6/2024

Principal 11/6/24