SYNERGY POLYTECHNIC, BBSR

The Lesson Plan

The Lesson Plan		·	
Descipline:COMPUTER SCIENCE	Semester:4TH		Name of the Teaching Faculty: SASWATI
& ENGINEERING			SANGHAMITRA PRADHAN
Subject:MICROPROCESSOR	No of Days/per		Semester from Date: 16/01/2024 to Date: 26/04/2024
AND MICROCONTROLLER	week class		No of Weeks:15
	allotted:5		
		NO. of	
Week	Class Day	class	Theory/Practical Topics
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			Unit-1:
			Microprocessor (Architecture and Programming-8 bit-8085)
			1.1 Introduction to Microprocessor and Microcomputer &
	1st	1	distinguish between them.
			4.2.Compared of Address born data have a surface born Born
	2nd	2	1.2 Concept of Address bus, data bus, control bus & System Bus
1st	3rd	3	1.3 General Bus structure Blockdiagram.
	4th	4	1.4 Basic Architecture of 8085 (8 bit) Microprocessor
			4.42
	5th	5	1.4 Basic Architecture of 8085 (8 bit) Microprocessor
			1.5 Signal Description (Pin diagram) of 8085 Microprocessor
73	1st	6	1
			1.5 Signal Description (Pin diagram) of 8085 Microprocessor
	2nd	7	- F
2nd			1.6 Register Organizations, Distinguish between SPR & GPR,
	3rd	8	Timing & Control, Module
,			1.6 Register Organizations, Distinguish between SPR & GPR,
	4th	9	Timing & Control, Module
	5th	10	1.7 Stack, Stack pointer & Stack top.
		1	
	1st	11	1.8 Interrupts:-8085 Interrupts, Masking of Interrupt(SIM,RIM)
	2nd	12	1.8 Interrupts:-8085 Interrupts, Masking of Interrupt(SIM,RIM)
3rd	3rd		
	Siu	13	revision
	4th	14	problem
		+	problem
	5th	15	class test
			Unit-2:
			Instruction Set and Assembly Language Programming
			2.1 Addressing data & Differentiate between one-byte, two-byte
	1st	16	&three-byte
	-	+	
	2nd	17	2.2 Addressing modes in instructions with the text
			2.2 Addressing modes in instructions with suitable examples

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4th	3rd	18	2.3 Instruction Set of 8085(Data Transfer, Arithmetic, Logic Branching, Stack & I/O, Machine Control) 2.4 Simple Assembly Language Programming of 8085
-, -		19	2.4.1 Simple Addition & Subtraction
	4th	20	2.4.2 Logic Operations (AND, OR, Complement 1's & 2's) & Masking of bits
	5th	21	2.4.3 Counters & Time delay (Single Register, Register Pair, More than Two Register)
	1st	22	2.4.4 Looping, Counting & Indexing (Call/JMP etc)
	2nd	23	2.4.5 Stack & Subroutinesprogrames.
5th	3rd	24	2.4.6 Code conversion, BCD Arithmetic & 16 Bit data Operation, Block Transfer.
	4th	25	2.4.7 Compare between two numbers
	5th	26	2.4.8 Array Handling (Largest number & smallest number in the array)
	1st	27	2.5 Memory & I/O Addressing.
6th	2nd	28	revision
	3rd	29	problem
	4th	30	class test

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Desciplina COMPUTED COUNTY	75 C		
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Week	Class Day		Theory/Practical Topics
			Unit-3: TIMING DIAGRAMS
		J	1.1 Define opcode, operand, T-State, Fetch cycle, Machine Cycle,
	1st		Instruction cycle & discuss the concept of timing diagram
			1.2 Draw timing diagram for memory read, memory write, I/O
	2nd		read, I/O write machine cycle
07th			1.2 Draw timing diagram for memory read, memory write, I/O
Í	3rd	33	read, I/O write machine cycle
			Draw a neat sketch for the timing diagram for 8085 instruction
	4th	34	(MOV,MVI,LDA instruction).
			Draw a neat sketch for the timing diagram for 8085 instruction
	5th	35	(MOV,MVI,LDA instruction).
			Draw a neat sketch for the timing diagram for 8085 instruction
	1st	36	(MOV,MVI,LDA instruction).
	2nd	37	problem
			Unit-4 Microprocessor Based System Development Aids
08th	3rd	38	4.1 Concept of interfacing
	-		4.2 Define Mapping &Data transfer mechanisms - Memory
	4th	39	mapping & I/O Mapping
Ą			4.3 Concept of Memory Interfacing:- Interfacing EPROM & RAM
	5th		Memories
	1st		4.4 Concept of Address decoding for I/O devices
	2nd	42	4.5 Programmable Peripheral Interface: 8255
09th	3rd		4.6 ADC & DAC with Interfacing.
	4th		4.7 Interfacing Seven Segment Displays
	5th	45	4.8 Generate square waves on all lines of 8255
		İ	
	1st	46	4.9 Design Interface a traffic light control system using 8255.
10th		ı	
1000	2nd	47	4.10 Design interface for stepper motor control using 8255.
	3rd	48	4.10 Design interface for stepper motor control using 8255.

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Principal

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Week	Class Day		Theory/Practical Topics
			Unit-5 Microprocessor (Architecture and Programming-16 bit-
	J		8086)
	1st	49	5.1 Register Organisation of 8086
=	2nd	50	5.2 Internal architecture of 8086
11th	3rd	51	5.3 Signal Description of 8086
	4th	52	5.4 General Bus Operation Physical Memory Organisation
	5th	53	5.5 Minimum Mode &Timings,
4	1st	54	5.6 Maximum Mode &Timings,
		55	5.7 Interrupts and Interrupt Service Routines, Interrupt Cycle,
	2nd	55	Non-Maskable Interrupt, Maskable Interrupt
l			
1	1 ,	56	5.8 8086 Instruction Set & Programming: Addressing Modes,
12th	3rd	l	Instruction Set, Assembler Directives and Operators
	, J	57	5.8 8086 Instruction Set & Programming: Addressing Modes,
,	4th		Instruction Set, Assembler Directives and Operators
1		58	5.9 Simple Assembly language programming using 8086
	5th	56	instructions.
		59	5.9 Simple Assembly language programming using 8086
434	1st	25	instructions.
13th	- 1	60	5.7 Interrupts and Interrupt Service Routines, Interrupt Cycle,
	2nd	00	Non-Maskable Interrupt, Maskable Interrupt
	,	64	Unit-6 Microcontroller (Architecture and Programming-8 bit):-
	1st	65	6.1 Distinguish between Microprocessor & Microcontroller
	2nd	66	6.2 8 bit & 16 bit microcontroller
14th	3rd	67	6.3 CISC & RISC processor
	4th	68	6.4 Architectureof8051Microcontroller
	5th	69	6.5 Signal Descriptionof8051Microcontrollers
	1st	70	6.6 Memory Organisation-RAM structure, SFR
	2nd	71	6.7 Registers, timers, interrupts of 8051 Microcontrollers
=	3rd	72	6.8 Addressing Modes of 8051
15th			6.9 Simple 8051 Assembly Language Programming Arithmetic&
	Ţ	73	Logic Instructions , JUMP, LOOP, CALL Instructions, I/O Port
	4th	1	Programming
-	5th	74	6.10Interrupts, Timer & Counters
	1st	75	programming
	2nd	76	programming
16th	3rd	77	programming
Part year	4th	78	programming
	5th	79	programming
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Principal Principal