

# Synergy Polytechnic, Bhubaneswar

## The Lesson Plan

|   |                                       |   |
|---|---------------------------------------|---|
| Discipline: Electrical Engineering            | Semester: 5th                         | Name of the Teaching Faculty: Satyabrata Pradhan  |
| Subject: Digital Electronics & Microprocessor | No of Days/per week class allotted: 5 | Semester from Date: 01/08/2023 to Date:<br>No of Weeks: 15  |
| Week  | Class Day                             | Theory/Practical Topics   |
| 1st   | 1st                                   | <b>BASICS OF DIGITAL ELECTRONICS:</b> Binary, Octal, Hexadecimal number systems and compare with Decimal system |
|   | 2nd                                   | Binary, Octal, Hexadecimal number systems and compare with Decimal system                                       |
|   | 3rd                                   | Binary addition, subtraction, Multiplication and Division   |
|   | 4th                                   | 1's complement and 2's complement numbers for a binary number   |
|   | 5th                                   | Subtraction of binary numbers in 2's complement method  |
| 2nd   | 1st                                   | Use of weighted and Un-weighted codes & write Binary equivalent number for a number in 8421,                    |
|   | 2nd                                   | Excess-3 and Gray Code and vice-versa.  |
|   | 3rd                                   | Importance of parity Bit  |
|   | 4th                                   | Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table   |
|   | 5th                                   | Realize AND, OR, NOT operations using NAND, NOR gates.  |
| 3rd   | 1st                                   | Different postulates and De-Morgan's theorems in Boolean algebra  |
|   | 2nd                                   | Use Of Boolean Algebra For Simplification Of Logic Expression   |
|   | 3rd                                   | Karnaugh Map For 2,3,4 Variable   |
|   | 4th                                   | Simplification Of SOP And POS Logic Expression Using K-Map  |
|   | 5th                                   | Simplification Of SOP And POS Logic Expression Using K-Map  |
| 4th   | 1st                                   | <b>COMBINATIONAL LOGIC CIRCUITS:</b> Give the concept of combinational logic circuits                           |
|   | 2nd                                   | Half adder circuit and verify its functionality using truth table   |
|   | 3rd                                   | Realize a Half-adder using NAND gates only and NOR gates only.  |
|   | 4th                                   | Full adder circuit and explain its operation with truth table   |
|   | 5th                                   | Realize full-adder using two Half-adders and an OR – gate and write truth table                                 |
| 5th   | 1st                                   | Full subtractor circuit and explain its operation with truth table.   |
|   | 2nd                                   | Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer   |
|   | 3rd                                   | Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer   |
|   | 4th                                   | Working of Binary-Decimal Encoder & 3 X 8 Decoder.  |

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| Week  | Class Day                             | Theory/Practical Topics  |
| 1st   | 1st                                   | Working of Two bit magnitude comparator  |
|   | 2nd                                   | Working of Two bit magnitude comparator  |
|   | 3rd                                   | problem practice   |
|   | 4th                                   | problem practice   |
|   | 5th                                   | problem practice   |
| 2nd   | 1st                                   | <b>3. SEQUENTIAL LOGIC CIRCUITS:</b> Give the idea of Sequential logic circuits.         |
|   | 2nd                                   | State the necessity of clock and give the concept of level clocking and edge triggering, |
|   | 3rd                                   | Clocked SR flip flop with preset and clear inputs.                                       |
|   | 4th                                   | Construct level clocked JK flip flop using S-R flip-flop and explain with truth table    |
|   | 5th                                   | Concept of race around condition and study of master slave JK flip flop.                 |
| 3rd   | 1st                                   | Give the truth tables of edge triggered D and T flip flops and draw their symbols.       |
|   | 2nd                                   | Applications of flip flops   |
|   | 3rd                                   | Define modulus of a counter  |
|   | 4th                                   | 4-bit asynchronous counter and its timing diagram.                                       |
|   | 5th                                   | Asynchronous decade counter.   |
| 4th   | 1st                                   | 4-bit synchronous counter  |
|   | 2nd                                   | Distinguish between synchronous and asynchronous counters.                               |
|   | 3rd                                   | State the need for a Register and list the four types of registers.                      |
|   | 4th                                   | Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop              |
|   | 5th                                   | Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop              |
| 5th   | 1st                                   | <b>4. 8085 MICROPROCESSOR:</b> Introduction to Microprocessors, Microcomputers           |
|   | 2nd                                   | Architecture of Intel 8085A Microprocessor and description of each block.                |
|   | 3rd                                   | Pin diagram and description.   |
|   | 4th                                   | Architecture of Intel 8085A Microprocessor and description of each block.                |
|   | 5th                                   | Pin diagram and description.   |

Sign of Faculty

HOD

Principal

26/7/23



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| 1st   | 1st                                   | Stack, Stack pointer & stack top   |
|   | 2nd                                   | Interrupts   |
|   | 3rd                                   | Opcode & Operand,  |
|   | 4th                                   | Differentiate between one byte, two byte & three byte instruction with example                         |
|   | 5th                                   | Instruction set of 8085 example  |
| 2nd   | 1st                                   | Addressing mode  |
|   | 2nd                                   | Addressing mode  |
|   | 3rd                                   | Fetch Cycle, Machine Cycle, Instruction Cycle, T-State   |
|   | 4th                                   | Fetch Cycle, Machine Cycle, Instruction Cycle, T-State   |
|   | 5th                                   | Timing Diagram for memory read, memory write, I/O read, I/O write                                      |
| 3rd   | 1st                                   | Timing Diagram for memory read, memory write, I/O read, I/O write                                      |
|   | 2nd                                   | Timing Diagram for 8085 instruction  |
|   | 3rd                                   | Counter and time delay   |
|   | 4th                                   | Simple assembly language programming of 8085   |
|   | 5th                                   | Simple assembly language programming of 8085   |
| 4th   | 1st                                   | Basic Interfacing Concepts, Memory mapping & I/O mapping   |
|   | 2nd                                   | Basic Interfacing Concepts, Memory mapping & I/O mapping   |
|   | 3rd                                   | Basic Interfacing Concepts, Memory mapping & I/O mapping   |
|   | 4th                                   | Functional block diagram and description of each block of Programmable peripheral interface Intel 8255 |
|   | 5th                                   | Functional block diagram and description of each block of Programmable peripheral interface Intel 8255 |
| 5th   | 1st                                   | Functional block diagram and description of each block of Programmable peripheral interface Intel 8255 |
|   | 2nd                                   | Application using 8255: Seven segment LED display, Square wave generator, Traffic light Contr          |
|   | 3rd                                   | Application using 8255: Seven segment LED display, Square wave generator, Traffic light Contr          |
|   | 4th                                   | Application using 8255: Seven segment LED display, Square wave generator, Traffic light Contr          |
|   | 5th                                   | Application using 8255: Seven segment LED display, Square wave generator, Traffic light Contr          |

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